



ibm memory optimization profiling statistics "cache misses" 1980 - 2002 Search

- ☒ Search only in: ☒ Business, Administration, Finance, and Economics  
☒ Engineering, Computer Science, and Mathematics  
☐ Search in all subject areas.

**Scholar** All articles Recent articles Results 1 - 100 of about 174 for ibm **memory optimization profiling** st

#### All Results

[K Pettis](#)

[D Burger](#)

[J Singh](#)

[R Hansen](#)

[T Austin](#)

#### Profile guided code positioning - group of 3 »

K Pettis, RC Hansen - Proceedings of the ACM SIGPLAN 1990 conference on ..., 1990 - portal.acm.org

... 1. Introduction Traditional **optimization** techniques attempt to improve pro ... page faults for virtual **memory** machines ... the support for basic block **profiling** and the ...

Cited by 347 - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

#### Optimization of instruction fetch mechanisms for high issue rates - group of 4

»

TM Conte, KN Menezes, PM Mills, BA Patel - Computer Architecture, 1995. Proceedings. 22nd Annual ..., 1995 - ieeexplore.ieee.org

... the six instruction per cycle **IBM POWER2** architecture ... The effect of com- piler **optimization** is analyzed to ... assumes that the instruction **memory** bandwidth into ...

Cited by 121 - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

#### End-user tools for application performance analysis using hardware counters - group of 7 »

K London, J Dongarra, S Moore, P Mucci, K Seymour, ... -International Conference on Parallel and Distributed ..., 2001 - cs.utk.edu

... SvPablo, being developed at the **IBM Advanced Computing** ... point instructions as the **profiling** metric. ... on single processor and shared **memory optimization** techniques ...

Cited by 44 - [Related Articles](#) - [View as HTML](#) - [Web Search](#)

#### Memory behavior of the SPEC2000 benchmark suite - group of 3 »

S Sair, M Charney - **IBM TJ Watson Research Center Technical Report**, 2000 - cs.ucsd.edu  
... ssair@cs.ucsd.edu mark.charney@us.ibm.com ... language compiler mcf C 190 Combinatorial

**optimization** crafty C 2.1 ... computing the **memory** component of the cycles per ...

Cited by 55 - [Related Articles](#) - [View as HTML](#) - [Web Search](#)

#### Dynamic and transparent binary translation - group of 7 »

M Gschwind, ER Altman, S Sathaye, P Ledak, D ... - Computer, 2000 - ieeexplore.ieee.org

... Paul Ledak David Appenzeller **IBM Burlington** ... Dynamic **optimization** can open new **optimization** opportunities ... nine different execution units: two **memory**, four integer ...

Cited by 65 - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

#### Portable profiling and tracing for parallel, scientific applications using C++ - group of 3 »

S Shende, AD Malony, J Cuny, P Beckman, S Karmesin ... - Proceedings of the SIGMETRICS symposium on Parallel and ..., 1998 - portal.acm.org

... of execution: "multi-threaded, shared **memory**" and "single ... in the presence of **optimization**, and portability. ... to limit traces to specified **profile** groups. ...

Cited by 72 - [Related Articles](#) - [Web Search](#)

Continuous program optimization: Design and evaluation - group of 8 »

T Kistler, M Franz - Computers, IEEE Transactions on, 2001 - [ieeexplore.ieee.org](http://ieeexplore.ieee.org)  
... into account the costs of **optimization** and **profiling**. ... AND FRANZ: CONTINUOUS PROGRAM

**OPTIMIZATION: DESIGN AND** ... the data-layout for **memory** intensive programs is ...

Cited by 68 - [Related Articles](#) - [Web Search](#) - [Library Search](#) - [BL Direct](#)

The SimpleScalar tool set, version 2.0 - group of 104 »

D Burger, TM Austin - ACM SIGARCH Computer Architecture News, 1997 - [portal.acm.org](http://portal.acm.org)  
... desired compile flags (eg, the correct **optimization** level ... c, =yscall.c, **memory.c**,  
regs\_c, loader.c, sc ... pester <star> generate a text-based **profile**, as described ...

Cited by 971 - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

A scalable cross-platform infrastructure for application performance tuning using hardware counters - group of 13 »

S Browne, J Dongarra, N Garner, K London, P Mucci - Proceedings of Supercomputing, November, 2000 - [doi.ieeecomputersociety.org](http://doi.ieeecomputersociety.org)  
... [4] David Cortesi, Origin 2000 and Onyx2 Performance Tuning and **Optimization** Guide. ... IBM RS/6000 Division, May 1999. ... **Memory** hierarchy access events ...

Cited by 94 - [Related Articles](#) - [Web Search](#)

Method for estimating statistics of properties of memory system transactions - group of 3 »

JA Dean, JE Hicks Jr, CA Waldspurger, WE Wehl - US Patent 6,332,178, 2001 - Google Patents

... to Support **Profile-Driven Optimization**, Proceedings of the ... IBM Technical Disclosure Bulletin, "Automatic Program ... related to specific **memory** transactions, such ...

Cited by 3 - [Related Articles](#) - [Web Search](#)

Apparatus and method for monitoring a computer system to guide optimization - group of 2 »

JA Dean, JE Hicks Jr, GZ Chrysos, CA Waldspurger, ... - US Patent 6,374,367, 2002 - Google Patents

... Data References in Unified Cache", IBM Technical Disclosure ... such as instructions, or **memory** references, or ... state information is analyzed to guide **optimization**. ...

Cited by 5 - [Related Articles](#) - [Web Search](#)

Profile-directed restructuring of operating system code - group of 6 »

WJ Schmidt, RR Roediger, CS Mestad, B Mendelson, I ... - IBM Systems Journal, 1998 - [research.ibm.com](http://research.ibm.com)

... on other platforms within IBM, we began ... better advantage of the **memory** paging system ...

process: instrumentation, benchmarking, and feedback-directed **optimization**. ...

Cited by 27 - [Related Articles](#) - [Cached](#) - [Web Search](#) - [BL Direct](#)

Method for estimating statistics of properties of memory system interactions among contexts in a ... - group of 3 »

JA Dean, CA Waldspurger - US Patent 6,237,059, 2001 - Google Patents

... to Support **Profile-Driven Optimization**, Proceedings of the ... IBM Technical Disclosure Bulletin, "Technique for Specu ... related to specific **memory** transactions, such ...

Cited by 2 - [Related Articles](#) - [Web Search](#)

Method for scheduling contexts based on statistics of memory system interactions in a computer ... - group of 2 »

JA Dean, CA Waldspurger - US Patent 6,442,585, 2002 - Google Patents  
 ... to Support **Profile-Driven Optimization**, Proceedings of ... **IBM** Technical Disclosure  
 Bulletin,  
 "Processor Performance ... related to specific **memory** transactions, such ...  
[Cited by 4](#) - [Related Articles](#) - [Web Search](#)

**Performance Analysis Using the MIPS R10000 Performance Counters - group of 13 »**

M Zagha, B Larson, S Turner, M Itzkowitz - Supercomputing, 1996. Proceedings of the 1996  
 ACM/IEEE ..., 1996 - [ieeexplore.ieee.org](#)  
 ... such as the Intel Pentium [16], **IBM** Power2 [14 ... to enable common subexpression  
 elimination of **memory** references ... improvements from loop nest **optimization** and inter ...  
[Cited by 162](#) - [Related Articles](#) - [Web Search](#)

**Examination of a **memory** access classification scheme for pointer-intensive and numeric programs - group of 7 »**

L Harrison - Proceedings of the 10th international conference on ..., 1996 - [portal.acm.org](#)  
 ... Wood used their CProf cache **profiling** system to ... programs are compiled with standard  
**optimization**, and the ... generates the contents of all **memory** locations that ...  
[Cited by 50](#) - [Related Articles](#) - [Web Search](#)

**Profile-guided post-link stride prefetching - group of 3 »**

CK Luk, R Muth, H Patil, R Weiss, PG Lowney, R ... - Proceedings of the 16th international  
 conference on ..., 2002 - [portal.acm.org](#)  
 ... compilers (eg, the **IBM** 5) and HP 30 ... of allocation for other objects, the **memory** lay-  
 out in ... also illustrates the following two opportunities for **optimization**. ...  
[Cited by 10](#) - [Related Articles](#) - [Web Search](#)

**Cache-efficient wavelet lifting in JPEG 2000 - group of 2 »**

S Chatterjee, CD Brooks - Multimedia and Expo, 2002. ICME'02. Proceedings. 2002 IEEE ...,  
 2002 - [ieeexplore.ieee.org](#)  
 ... Christopher D. Brooks **IBM** Software Group 3901 S ... Version 4.2, using the **optimization**  
 flag -fast ... obtained instruction counts and **memory statistics** through execution ...  
[Cited by 12](#) - [Related Articles](#) - [Web Search](#)

**Contrasting characteristics and cache performance of technical and multi-user commercial workloads**

AMG Maynard, CM Donnelly, BR Olszewski - ACM SIGPLAN Notices, 1994 - [portal.acm.org](#)  
 ... was not traced if the software **profile** of an ... applications that would have larger **memory**  
 requirements (and ... The traces were collected on several **IBM** RISC System ...  
[Cited by 149](#) - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

**The Influence of Caches on the Performance of Sorting - group of 21 » •**

A LaMarca, RE Ladner - Journal of Algorithms, 1999 - Elsevier  
 ... well as to keep long term **statistics** on cache ... Thus, the number of **cache misses** per  
 key in ... Multiquicksort employs a second **memory optimization** in similar spirit ...  
[Cited by 115](#) - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

**SPAIID: software prefetching in pointer-and call-intensive environments - group of 7 »**

MH Lipasti, WJ Schmidt, SR Kunkel, RR Roediger - Proceedings of the 28th annual  
 international symposium on ..., 1995 - [portal.acm.org](#)  
 ... methods to improve paging behavior of main **memory** [HG71, Fer74 ... completion and  
 were  
 compiled with the **IBM** XL family ... and XIC for C) at full **optimization** under AIX ...

[Cited by 90](#) - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

**Profiling I/O interrupts in modern architectures - group of 8 »**

L Schaelicke, A Davis, SA McKee - Modeling, Analysis and Simulation of Computer and ..., 2000 - [ieeexplore.ieee.org](#)

**Profiling** YO Interrupts in Modern Architectures ... Intel Pentium-Pro [2], MIPS R10000/R12000 [ 131, **IBM** Power2 [22 ... a large file (equal to the main **memory** size of ...

[Cited by 8](#) - [Related Articles](#) - [Web Search](#)

**SPLASH: Stanford parallel applications for shared-memory - group of 7 »**

JP Singh, WD Weber, A Gupta - ACM SIGARCH Computer Architecture News, 1992 - [portal.acm.org](#)

... Systems 1.31) compilers, using the -O2 level of **optimization**. ... altering the interactions with the **memory** system on ... program structure and **profiling** information. ...

[Cited by 778](#) - [Related Articles](#) - [Web Search](#)

**Integrating Fine-Grained Message Passing in Cache Coherent Shared Memory Multiprocessors - group of 11 »**

DK Poulsen, PC Yew - Journal of Parallel and Distributed Computing, 1996 - [citeseer.csail.mit.edu](#)

... the National Security Agency, and an **IBM** Resident Study ... This type of **optimization** can be especially useful ... **memory** modules, are full-mapped, and are organized ...

[Cited by 8](#) - [Related Articles](#) - [View as HTML](#) - [Web Search](#) - [BL Direct](#)

**A performance methodology for commercial servers - group of 5 »**

SR Kunkel, RJ Eickemeyer, MH Lipasti, TJ Mullins, ... - **IBM** Journal of Research and Development, 2000 - [research.ibm.com](#)

... or cycle time), and for software **optimization**, including compiler ... that access the system's main **memory** at high ... **IBM** servers address these requirements using the ...

[Cited by 18](#) - [Related Articles](#) - [Cached](#) - [Web Search](#) - [BL Direct](#)

**Understanding why correlation profiling improves the predictability of data cache misses in ... - group of 5 »**

TC Mowry, CK Luk - Computers, IEEE Transactions on, 2000 - [ieeexplore.ieee.org](#)

... numbered nodes are adjacent in **memory**.) (a) Example ... each application with -O2 **optimization** using the ... LUK: UNDERSTANDING WHY CORRELATION PROFILING IMPROVES THE ...

[Cited by 1](#) - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

**Run-time cache bypassing - group of 14 »**

TL Johnson, DA Connors, MC Merten, WW Hwu - IEEE Transactions on Computers, 1999 - [doi.ieeeecs.org](#)

... The **profiling** results for a 100,000-cycle sample of ... implementation of the cache bypassing **optimization** was presented ... choices are made by a **Memory** Address Table ...

[Cited by 28](#) - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

**A Portable Programming Interface for Performance Evaluation on Modern Processors - group of 16 »**

S Browne, J Dongarra, N Garner, G Ho, P Mucci - International Journal of High Performance Computing ..., 2000 - [hpc.sagepub.com](#)

... being developed at the **IBM** Advanced Computing ... parallelization, OpenMP) and distributed-memory (MPI, HPF ... **profiling** analysis, and relating **profiling** results to ...

[Cited by 146](#) - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

Unified compilation techniques for shared and distributed address space machines - group of 3 »

CW Tseng, JM Anderson, SP Amarasinghe, MS Lam - Proceedings of the 9th international conference on ..., 1995 - portal.acm.org

... the Intel Paragon, Thinking Machines CM-5, and **IBM SP-2** ... **Cache Misses** There are two

kinds of **memory** subsystem **optimization** techniques: minimizing **cache** ...

[Cited by 16](#) - [Related Articles](#) - [Web Search](#)

BOA: The Architecture of a Binary Translation Processor - group of 6 »

E Altman, M Gschwind, S Sathaye... - Research Report RC21665, **IBM TJ Watson Research Center**, ..., 2000 - research.ibm.com

... is an implementation of the **IBM POWER** processor ... Load/store telescoping eliminates dependencies through **memory**. ... **optimization** opens new **optimization** opportunities ...

[Cited by 13](#) - [Related Articles](#) - [View as HTML](#) - [Web Search](#)

Whole-program **optimization** for time and space efficient threads - group of 5

»

D Grunwald, R Neves - Proceedings of the seventh international conference on ..., 1996 - portal.acm.org

... **ibm**. ... We think it's still likely that the context switch **optimization** will be ... Although dynamic **memory** allocation is usually considered to be significantly more ...

[Cited by 21](#) - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

Method for estimating **statistics** of properties of interactions processed by a processor pipeline - group of 3 »

J Dean, JE Hicks, SC Root, CA Waldspurger, WE ... - US Patent 6,119,075, 2000 - Google Patents

... of Program Counter Sampling, **IBM Technical Disclosure** ... to Support **Profile-Driven Optimization**, Proceedings of the ... et al., Informing **Memory** Operations: Providing ...

[Cited by 8](#) - [Related Articles](#) - [Web Search](#)

[book] Performance Debugging and Tuning Using an Instruction-set Simulator - group of 8 »

PS Magnusson, J Montelius - 1997 - citeseer.csail.mit.edu

... examples. 3.1 **Profiling** A profiler gathers and presents **statistics** that are related to a **memory** address range. A ...

[Cited by 5](#) - [Related Articles](#) - [View as HTML](#) - [Web Search](#) - [Library Search](#)

Method for providing virtual **memory** to physical **memory** page mapping in a computer operating system ... - group of 3 »

J Dean, JE Hicks Jr, WE Weihl - US Patent 6,237,073, 2001 - Google Patents

... 79-81. **IBM Technical Disclosure Bulletin**, "Instruction Match Function for Processor Performance Monitoring", Dec. ... 710 \SAMPLE **MEMORY** INTERACTION ... **PROFILE RECORD** ...

[Cited by 5](#) - [Related Articles](#) - [Web Search](#)

Dynamic binary translation and **optimization** - group of 10 »

K Ebcioglu, E Altman, M Gschwind, S Sathaye - Computers, IEEE Transactions on, 2001 - ieeexplore.ieee.org

... with reasonable translation overhead and **memory** usage. ... compilation, binary translation,

dynamic **optimization**, just-in ... The authors are with the **IBM TJ.Watson** ...

[Cited by 42](#) - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

[Profile-Based Energy Reduction in High-Performance Processors - group of 16 »](#)

M Huang, J Renau, J Torrellas - ... ACM Workshop on Feedback-Directed and Dynamic Optimization, 2001 - ece.rochester.edu

... The architecture loosely models an **IBM** Power3 chip ... cache [18] in the instruction **memory** hierarchy. ... the IRIX MIPSPro compiler version 7.3 with -O2 **optimization**. ...

[Cited by 12](#) - [Related Articles](#) - [View as HTML](#) - [Web Search](#)

[Increasing the accuracy of statistical simulation for modeling superscalar processors - group of 2 »](#)

L Eeckhout, K De Bosschere - Performance, Computing, and Communications, 2001. IEEE ..., 2001 - ieeexplore.ieee.org

... the synthetic trace matches the statistical **profile** of the ... D-cache access time or a main **memory** access time ... compiler version 5.6 with the **optimization** flag set ...

[Cited by 2](#) - [Related Articles](#) - [Web Search](#)

[Code transformations to improve memory parallelism - group of 21 »](#)

VS Pai, S Adve - Microarchitecture, 1999. MICRO-32. Proceedings. 32nd Annual ..., 1999 - ieeexplore.ieee.org

... supported in part by an **IBM** Partnership award ... leading references can overestimate **memory** parallelism, since ... be measured through cache simulation or **profiling**. ...

[Cited by 27](#) - [Related Articles](#) - [Web Search](#)

[Binary translation and architecture convergence issues for IBM system/390 - group of 4 »](#)

M Gschwind, K Ebcioglu, E Altman, S Sathaye - Proceedings of the 14th international conference on ..., 2000 - portal.acm.org

... point unit, since IEEE floating point subsumes the capabilities of **IBM** floating point ... A special **optimization** is applicable to short **memory-to-memory** ...

[Cited by 10](#) - [Related Articles](#) - [Web Search](#)

[Reducing indirect function call overhead in C++ programs - group of 12 »](#)

B Calder, D Grunwald - Proceedings of the 21st ACM SIGPLAN-SIGACT symposium on ..., 1994 - portal.acm.org

... Keywords: Object oriented programming, **optimization**, **profile-based optimization**, customization ... the address of the call target is loaded from **memory**. ...

[Cited by 126](#) - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

[Compilers for Instruction-Level Parallelism - group of 3 »](#)

WHY ILP - IEEE Micro, 1996 - doi.ieeecomputersociety.org

... Silicon Graphics Kemal Ebcioglu **IBM** TJ Watson ... exist for partial inlining and interprocedural **optimization**. ... penalties associated with **memory** latencies and **cache** ...

[Related Articles](#) - [Web Search](#)

[Strategies to Improve Performance in the IA64 Architecture](#)

G Teixeira - 2002 - gec.di.uminho.pt

... Processor Microarchitecture Reference for Software **Optimization**, Intel, Santa ... IA-64 rollout - Virtual **memory**, Interrupts more ... 8] Hopkins, M., **IBM** Research, A ...

[Cited by 1](#) - [Related Articles](#) - [View as HTML](#) - [Web Search](#)

[Cache behavior of network protocols - group of 3 »](#)

E Nahum, D Yates, J Kurose, D Towsley - Proceedings of the 1997 ACM SIGMETRICS international ..., 1997 - portal.acm.org

... suremcntGroupFellowship and is currently with the **IBM** TJ Watson ... network protocol processing,

deriving **statistics** such as ... focusing solely on the **memory** behavior of ...

[Cited by 21](#) - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

**Informing memory operations: memory performance feedback mechanisms and their applications - group of 11 »**

M Horowitz, M Martonosi, TC Mowry, MD Smith - ACM Transactions on Computer Systems (TOCS), 1998 - [portal.acm.org](#)

... by a Faculty Development Award from **IBM**. ... Programming Languages]: Processors—compilers;

**optimization** General Terms ... on a detailed **memory profile** captured from ...

[Cited by 19](#) - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

**HPCVIEW: A Tool for Top-down Analysis of Node Performance - group of 7 »**

J Mellor-Crummey, RJ Fowler, G Marin, N Tallent - The Journal of Supercomputing, 2001 - Springer

... of floating point operations to **memory** references within ... line instance information with raw **profile** data will ... the code generated at each level of **optimization**. ...

[Cited by 39](#) - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

**LimitLESS directories: A scalable cache coherence scheme - group of 21 »**

D Chaiken, J Kubiawicz, A Agarwal - Proceedings of the fourth international conference on ..., 1991 - [portal.acm.org](#)

... ducing network traffic and average **memory** access latency. ... the performance of a full-map directory with the **memory** overhead of a limited directory. ...

[Cited by 209](#) - [Related Articles](#) - [Web Search](#) - [Library Search](#)

**Evaluating non-deterministic multi-threaded commercial workloads - group of 8 »**

AR Alameldeen, CJ Mauer, M Xu, PJ Harper, MM ... - Proceedings of the Fifth Workshop on Computer Architecture ..., 2002 - [cae.wisc.edu](#)

... Sun's WorkShop C 6.1 with aggressive **optimization**. ... by introducing minor perturbations in **memory** system latencies ... and CCR-0105721, an **IBM** Graduate Fellowship ...

[Cited by 28](#) - [Related Articles](#) - [View as HTML](#) - [Web Search](#)

**The PAPI Cross-Platform Interface to Hardware Performance Counters - group of 3 »**

K London, S Moore, P Mucci, K Seymour, R Luczak - Department of Defense Users' Group Conference Proceedings, ..., 2001 - [cs.utk.edu](#)

... is planned on the **IBM** Power3 SMP. ... The **memory** utilization extension is expected to be ... Infrastructure for Application Performance **Optimization** Using Hardware ...

[Cited by 14](#) - [Related Articles](#) - [View as HTML](#) - [Web Search](#)

**Analyzing and tuning memory performance in sequential and parallel programs - group of 4 »**

MR Martonosi - 1993 - [reports.stanford.edu](#)

... 2.2.1 Data and Code Oriented **Statistics** : : : : 19 2.2.2 **Memory Statistics** on Causes of **Cache Misses** : : : : 20 ...

[Cited by 11](#) - [Related Articles](#) - [View as HTML](#) - [Web Search](#) - [Library Search](#)

**Performance issues in correlated branch prediction schemes - group of 15 »**

N Gloy, MD Smith, C Young - Proceedings of the 28th annual international symposium on ..., 1995 - [portal.acm.org](#)

... of object code size on instruction **memory** performance ... control flow graphs, and the **profile** information are ... cc version 2.0.0 and the **optimization** level specified ...

[Cited by 12](#) - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

**Online feedback-directed optimization of Java - group of 21 »**

M Arnold, M Hind, BG Ryder - Proceedings of the 17th ACM SIGPLAN conference on Object-  
..., 2002 - portal.acm.org

... To keep overhead low, the IBM DK 1.3.0 [43, 44 ... For example, recording all **memory** refer-  
ences [19] or ... Exception Directed **Optimization** (EDO) [38] also adds in ...

[Cited by 49](#) - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

**Scalable Analysis Techniques for Microprocessor Performance Counter Metrics - group of 18 »**

DH Ahn, JS Vetter - Supercomputing, ACM/IEEE 2002 Conference, 2002 -  
ieeexplore.ieee.org

... for refining their code **optimization** efforts. ... main **memory** for a total of 64 GB system  
**memory**. A Colony SPSwitch—a proprietary **IBM** interconnect— connects the ...

[Cited by 32](#) - [Related Articles](#) - [Web Search](#)

**ONLINE PROFILING AND FEEDBACK-DIRECTED OPTIMIZATION OF JAVA - group of 8 »**

M ARNOLD - 2002 - cs.rutgers.edu

... 94 IBM DK 1.3.0 . . . . . 94 Hotspot . . . . . Performing  
**profiling** and **optimization** online, during ...

[Cited by 8](#) - [Related Articles](#) - [View as HTML](#) - [Web Search](#) - [Library Search](#)

**Memory hierarchy synthesis of a multimedia embedded processor - group of 4 »**

ST Fu, DF Zucker, MJ Flynn - Computer Design: VLSI in Computers and Processors, 1996.  
..., 1996 - ieeexplore.ieee.org

... (TI, IBM, AT&T) Of ... Maximum **optimization** was set using the +03 option. ... code so  
that

ex- ternal library functions are called for every **memory** access instruction. ...

[Cited by 3](#) - [Related Articles](#) - [Web Search](#)

**System-level power optimization: techniques and tools - group of 17 »**

L Benini, G de Micheli - ACM Transactions on Design Automation of Electronic Systems ...,  
2000 - portal.acm.org

... If decompression had required off-chip **memory** access, MPEG ... From **profiling**, the  
main

computational kernels are extracted ... System-Level Power **Optimization** • 127 ...

[Cited by 225](#) - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

**Modeling and Analyzing CPU Power and Performance: Metrics, Methods, and Abstractions - group of 2 »**

M Martonosi, D Brooks, P Bose - SIGMETRICS 2001/Performance 2001-Tutorials, 2001 -  
ee.princeton.edu

... **optimization** □ Trade off parallelism against clock frequency ... Princeton Wattch □

**IBM** PowerTimer ... Table-lookup based power models for **memory** and ...

[Cited by 11](#) - [Related Articles](#) - [View as HTML](#) - [Web Search](#)

**Better Global Scheduling Using Path Profiles - group of 12 »**

C Young, MD Smith - Proceedings of the 31st annual ACM/IEEE international ..., 1998 -  
doi.ieeecomputersociety.org

... the program and thus can hurt **memory** system performance. ... a Pettis and Hansen-style  
[15] procedure- placement **optimization**. ... 3.1 Efficient general path **profiling** ...



[Cited by 39](#) - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

**Program balance and its impact on high performance RISC architectures - group of 10 »**

LK John, V Reddy, PT Hulina, LD Coraor - High-Performance Computer Architecture, 1995. Proceedings. ..., 1995 - [ieeexplore.ieee.org](#)

... all **memory** refer- ences made by **IBM 360** programs ... with the highest level of **optimization**,

-04 and ... on address arithmetic and overhead **memory** references performed ...

[Cited by 14](#) - [Related Articles](#) - [Web Search](#)

**Selective value prediction - group of 16 »**

B Calder, G Reinman, DM Tullsen - ACM SIGARCH Computer Architecture News, 1999 - [portal.acm.org](#)

... Table 1: Program **statistics** for the baseline architecture ... 16-way dynam- ically scheduled

microprocessor with two levels of instruc- tion and data cache **memory**. ...

[Cited by 147](#) - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

**Profile-based characterization and tuning for subsurface sensing and imaging applications - group of 4 »**

M Ashouei, D Jiang, W Meleis, D Kaeli, M El- ... - International Journal of Systems, Science and Technology, 2002 - [ducati.doc.ntu.ac.uk](#)

... is achieved on the 4-processor 667MHz Alpha shared-**memory** system ... **2 PROFILE-GUIDED**

**OPTIMIZATION Profiling** has been used to guide a number compilation and program ...

[Cited by 2](#) - [Related Articles](#) - [View as HTML](#) - [Web Search](#)

**The Importance of Prepass Code Scheduling for Superscalar and Superpipelined Processors - group of 21 »**

DM Lavery, PP Chang, SA Mahlke, WY Chen, WW Hwu - IEEE Transactions on Computers, 1995 - [doi.ieeecomputersociety.org](#)

... US Department of Energy and the **IBM** Corporation. ... **memory** access sequence control for

**memory** dependences ... general percolation rather than compiler **optimization** bugs ...

[Cited by 51](#) - [Related Articles](#) - [Web Search](#) - [Library Search](#) - [BL Direct](#)

**A VLIW architecture for a trace scheduling compiler - group of 15 »**

RP Colwell, RP Nix, JJ O'Donnell, DB Papworth, PK ... - IEEE Transactions on Computers, 1988 - [doi.ieeecs.org](#)

... In conjunc- tion with the global **optimization** ability of our ... Subsystem The speed of the CPU/**memory** interconnection in ... modern computer system, from the **IBM PC** to ...

[Cited by 375](#) - [Related Articles](#) - [Web Search](#)

**[book] A Framework for Data Prefetching Using Off-line Training of Markovian Predictors - group of 13 »**

J Kim, KV Palem, WF Wong - 2002 - Center for Research on Embedded Systems and Technology, College ...

... a new paradigm that utilizes extensive **profiling** and powerful off ... Research on **memory** hierarchy **optimization** can be clas ... The gap in **memory** and processor speed is ...

[Cited by 6](#) - [Related Articles](#) - [Web Search](#) - [Library Search](#)

**An overview of common benchmarks - group of 7 »**

RP Weicker - Computer, 1990 - [doi.ieeecs.org](#)

... the Fortran compiler's code **optimization** quality: For ... Size, procedure **profile**, and

language- feature distribution. ... parameters are allocated in **memory** in the ...  
[Cited by 43](#) - [Related Articles](#) - [Web Search](#)

#### Wisconsin Architectural Research Tool Set

MD Hill, JR Larus, AR Lebeck, M Talluri, DA Wood - ACM SIGARCH Computer Architecture News, 1993 - portal.acm.org  
 ... function entry and exit, and **memory** allocation and ... and James R. Larus, "Optimally **Profiling** and Tracing ... 2. Execution Time Speedup at **Optimization Level -03** ...  
[Cited by 25](#) - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

#### OPTIMIZING MEMORY-RESIDENT DECISION SUPPORT SYSTEM WORKLOADS FOR CACHE MEMORIES

PPM TRANCOSO - 1998 - historical.ncstrl.org  
 ... systems include Oracle 8 [13], **IBM's** DB2 [14] ... and those that do neglect the cache **memory**. ... Adapt existing blocking algorithm **optimization** for pipelined database ...  
[Related Articles](#) - [View as HTML](#) - [Web Search](#) - [Library Search](#)

#### A trace cache microarchitecture and evaluation - group of 25 »

E Rotenberg, S Bennett, JE Smith - IEEE Transactions on Computers, 1999 - doi.ieeecs.org  
 ... recognized the problem imposed by branches on code **optimization**. ... any unresolved stores,  
 and any **memory** hazards are ... Rotenberg is supported by an **IBM** Fellowship. ...  
[Cited by 60](#) - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

#### An Empirical Performance Evaluation of Scalable Scientific Applications - group of 18 »

JS Vetter, A Yoo - Supercomputing, ACM/IEEE 2002 Conference, 2002 - ieeexplore.ieee.org  
 ... on eight hardware counters in the **IBM** POWER3 processor ... **cache misses**, and number of  
**memory** loads and ... typically less sensitive to compiler **optimization** than other ...  
[Cited by 27](#) - [Related Articles](#) - [Web Search](#)

#### Architectural tradeoffs in the design of MIPS-X - group of 4 »

P Chow, M Horowitz - Proceedings of the 14th annual international symposium on ..., 1987 - portal.acm.org  
 ... reduced instruction set processors (**IBM** 8011 , RISC ... particularly for a previous **memory** fetch because ... we have since developed better **optimization** techniques and ...  
[Cited by 41](#) - [Related Articles](#) - [Web Search](#)

#### Apparatus for sampling instruction execution information in a processor pipeline - group of 3 »

GZ Chrysos, J Dean, JE Hicks, CA Waldspurger, WE ... - US Patent 6,195,748, 2001 - Google Patents  
 .. Using Branch Handling Hardware to Support **Profile-Driven Optimization**, Proceedings of ... **IBM** technical disclosure bulletin, US **IBM** Corp. ... **SAMPLE MEMORY INTERACTION** ...  
[Cited by 9](#) - [Related Articles](#) - [Web Search](#)

#### Factoring: a method for scheduling parallel loops - group of 3 »

SF Hummel, E Schonberg, LE Flynn - Communications of the ACM, 1992 - portal.acm.org  
 ... 11].run-time system for the **IBM** restructuring Fortran ... have been implemented on shared-  
**memory** multiprocessors [5 ... ance using **profiling** [15], we have chosen not ...  
[Cited by 205](#) - [Related Articles](#) - [Web Search](#)

**A Hierarchical Approach to Modeling and Improving the Performance of Scientific Applications on the ... - group of 9 »**

EL Boyd, W Azeem, HH Lee, TP Shih, SH Hung, ES ... - Proceedings of the 1994 International Conference on Parallel ..., 1994 - users.ece.gatech.edu  
... calculated by K-MA and **profile**-generated frequencies ... by taking weighted averages of the component **statistics**. ... an application and generates **memory** traces of ...  
[Cited by 16](#) - [Related Articles](#) - [View as HTML](#) - [Web Search](#) - [BL Direct](#)

**Profiling a Parallel Language Based on Fine-Grained Communication - group of 4 »**

B Haake, KE Schauser, CJ Scheiman - Supercomputing, 1996. Proceedings of the 1996 ACM/IEEE ..., 1996 - ieeexplore.ieee.org  
... over the recent years, including ParaGraph [HE91], PICL [GHPW90], **IBM's** VT ...  
**Memory** ...  
If barriers are very frequent, one simple **optimization** is to incorporate a ...  
[Cited by 4](#) - [Related Articles](#) - [Web Search](#)

**Apparatus for determining the instantaneous average number of instructions processed - group of 3 »**

GZ Chrysos, J Dean, JE Hicks Jr, CA Waldspurger, ... - US Patent 6,175,814, 2001 - Google Patents  
... **IBM** technical disclosure bulletin "Processor Performance Monitoring with a depiction of the efficiency of the cache ... **SAMPLE MEMORY INTERACTION ... PROFILE RECORD** 1, ...  
[Cited by 6](#) - [Related Articles](#) - [Web Search](#)

**Compiler and Microarchitecture Mechanisms for Exploiting Registers to Improve Memory Performance - group of 2 »**

MA Postiff - 2001 - eecs.umich.edu  
... now at **IBM**. ... Figure 3.18: Register requirements for go across several **optimization** levels. ... Figure 6.18: Code in compress that is responsible for **memory** activity ...  
[Cited by 6](#) - [Related Articles](#) - [View as HTML](#) - [Web Search](#) - [Library Search](#)

**[book] IBM SP User's Guide - group of 5 »**

J Haataja, T Kupila-Rantala - 2001 - stfx.ca  
... message-passing library, OpenMP shared **memory** standard and ... 9 on page 80 illustrates  
**IBM** programming tools ... parallel debugger pdbx and available **profiling** tools. ...  
[Related Articles](#) - [Web Search](#) - [Library Search](#)

**A Framework for Persistence-Enabled Optimization of Java Object Stores - group of 6 »**

D Whitlock, AL Hosking - Lecture Notes In Computer Science; Vol. 2135, 2000 - Springer  
... the Unix crypt utility db Operations on **memory**-resident database ... A Framework for Persistence-Enabled **Optimization** of Java ... Table 2. Inlining **statistics** (static) ...  
[Related Articles](#) - [Web Search](#) - [BL Direct](#)

**Compilers for instruction-level parallelism - group of 8 »**

M Schlansker, TM Conte, J Dehnert, K Ebcioglu, JZ ... - Computer, 1997 - ieeexplore.ieee.org  
... Silicon Graphics Kemal Ebcioglu **IBM** TJ Watson ... exist for partial inlining and interprocedural **optimization**. ... **Memory** refer- ences present especially important ...  
[Cited by 14](#) - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

**Multi-View Memory Support to Operating Systems in Locking for Transaction and Database Systems - group of 8 »**

P Bodorik, D Jutla - The Computer Journal, 1998 - Br Computer Soc

Page 1. Multi-View **Memory** Support to Operating Systems in Locking for Transaction and Database Systems P. B ODORIK 1 AND D. J UTLA 2 ... 2. MULTI-LEVEL **MEMORY** MODEL ...

[Cited by 2](#) - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

**A Case Study of 3 Internet Benchmarks on 3 Superscalar Machines - group of 4 »**

Y Luo, P Seshadri, J Rubio, L John, A Mericas - 2001 - ece.utexas.edu

... **IBM's** pmcount (a utility that allows the user to ... in turn, read the packet into a buffer in main **memory**. ... shows a similarly poor decode and retirement **profile**. ...

[Cited by 2](#) - [Related Articles](#) - [View as HTML](#) - [Web Search](#)

**Near-optimal intraprocedural branch alignment - group of 24 »**

C Young, DS Johnson, MD Smith, DR Karger - ACM SIGPLAN Notices, 1997 - portal.acm.org

... placement tech- niques can reduce instruction **cache misses** as well as ... level cache, and 128 MB of main **memory**. ... the time spent compiling and **profiling** under our ...

[Cited by 32](#) - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

**Method and apparatus for sampling multiple potentially concurrent instructions in a processor ... - group of 3 »**

GZ Chrysos, J Dean, JE Hicks, DL Leibholz, EJ ... - US Patent 6,163,840, 2000 - Google Patents

... a Symmetric Multiple Processor Envi- ronment," **IBM** TDB, vol. ... Handling Hardware to Support **Profile-Driven Optimization**, Proceedings of ... **SAMPLE MEMORY** INTERACTION ...

[Cited by 3](#) - [Related Articles](#) - [Web Search](#)

**DataScalar: A Memory-Centric Approach to Computing - group of 17 »**

S Kaxiras, D Burger, JR Goodman - Journal of Systems Architecture, 1999 - cs.utexas.edu

... extended periods waiting for off-chip **cache misses**, the **memory** ... fetched by some processor, and each **memory** update can ... is a mem- ory system **optimization**, not a ...

[Cited by 1](#) - [Related Articles](#) - [View as HTML](#) - [Web Search](#)

**HPCView: A Tool for Top-down Analysis of Node Performance - group of 2 »**

G MARIN, N TALLENT - The Journal of Supercomputing, 2002 - kluweronline.com

... of floating point operations to **memory** references within ... line instance information with raw **profile** data will ... the code generated at each level of **optimization**. ...

[Related Articles](#) - [Web Search](#)

**Design considerations for distributed caching on the Internet - group of 16 »**

R Tewari, M Dahlin, HM Vin, JS Kay - Distributed Computing Systems, 1999. Proceedings. 19th IEEE ..., 1999 - ieeexplore.ieee.org

... Award (CDA-9624082) and grants from **IBM**, Intel, Lucent ... 3 An obvious **optimization**, not currently implemented in our ... node's hint cache in a **memory** mapped file ...

[Cited by 271](#) - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

**An Object-Oriented Library for Shared-Memory Parallel Simulations - group of 5 »**

P Machanick - 1996 - it.uq.edu.au

... reducing **cache misses**. ... block aligned **memory** access to be a big win, and is more likely to be a ... **optimization** than blocking, across a variety of applications. ...  
[Cited by 2](#) - [Related Articles](#) - [View as HTML](#) - [Web Search](#)

[PS] Path-based Compilation - group of 8 »

RC Young - 1998 - cs.bell-labs.com  
 ... At **IBM** Research in Eric Kron- ... executed procedures. Other profilers [9, 64] have been used to examine **memory** traffic in ... more than is desirable for **optimization**. ...  
[Cited by 24](#) - [Related Articles](#) - [View as HTML](#) - [Web Search](#) - [Library Search](#)

On the value locality of store instructions - group of 10 »

KM Lepak, MH Lipasti - Proceedings of the 27th annual international symposium on ..., 2000 - portal.acm.org  
 ... benchmarks were compiled with the **IBM** AIX optimizing C ... tions, while the SimpleScalar **statistics** include speculative ... only a weakly consistent **memory** model, and ...  
[Cited by 58](#) - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

Silent stores for free: Reducing the cost of store verification - group of 3 »

KM Lepak - Master's thesis, University of Wisconsin-Madison, 2000 - ece.wisc.edu  
 ... of **memory** dependences is an **optimization** commonly implemented ... well as consistency models, **memory** traffic reduction ... Whitepaper, <http://www.rs6000.ibm.com>, 1999. ...  
[Cited by 2](#) - [Related Articles](#) - [View as HTML](#) - [Web Search](#)

Static correlated branch prediction - group of 8 »

C Young, MD Smith - ACM Transactions on Programming Languages and Systems ( ..., 1999 - portal.acm.org  
 ... AMD, Compaq, Digital Equipment, HP, **IBM**, and Intel ... machine because of the instruction **memory** resources consumed ... of both the **profiling** and **optimization** parts of ...  
[Cited by 19](#) - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

A Study of Cache Performance in Java Virtual Machines - group of 4 »

A Rajan - 2002 - lca.ece.utexas.edu  
 ... Adaptive **optimization** ... **memory**, and other platform specific features ... CLIPS rule-based expert systems 3. Db Data management benchmarking software written by **IBM**. ...  
[Cited by 2](#) - [Related Articles](#) - [View as HTML](#) - [Web Search](#) - [Library Search](#)

Transient fault detection via simultaneous multithreading - group of 19 »

SK Reinhardt, SS Mukherjee - ACM SIGARCH Computer Architecture News, 2000 - portal.acm.org  
 ... redundancy has become a common performance **optimization** for hardware ... with a consistent view of **memory**, the store ... register file (as in the **IBM** G5 microprocessor ...  
[Cited by 129](#) - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

Dynamic Optimization Infrastructure and Algorithms for IA-64

KM Hazelwood - 2000 - lib.ncsu.edu  
 ... 34 2.4 **Profiling** Monitors For Feedback-Directed **Optimization**.....35  
 2.4.1 ProfileMe ... base **optimization** on an average **profile**. ...  
[Cited by 1](#) - [Related Articles](#) - [View as HTML](#) - [Web Search](#)

Design issues and tradeoffs for write buffers - group of 12 »

K Skadron, DW Clark - Proceedings of the Third International Symposium on High- ..., 1997 - doi.ieeecomputersociety.org  
 ... but instead measure average cycles per **memory** reference. ... objects and doduc 1  
 Inter-file-**optimization** 2 Sets ... improvement of- ten requires cache **profiling** [16, ...  
[Cited by 47](#) - [Related Articles](#) - [Web Search](#)

Three architectural models for compiler-controlled speculative execution - group of 8 »

PP Chang, NF Warter, SA Mahlke, WY Chen, WW Hwu - IEEE Transactions on Computers, 1995 - doi.ieeecomputersociety.org  
 ... a conditional branch such as in the **IBM 360/91** ... trapping and non-trapping versions for **memory** loads, integer ... to the areas of compiler **optimization** and computer ...  
[Cited by 31](#) - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

An analysis of operating system behavior on a simultaneous multithreaded architecture - group of 15 »

JA Redstone, SJ Eggers, HM Levy - ACM SIGPLAN Notices, 2000 - portal.acm.org  
 ... of cycles in the Apache workload.) Another possible **optimization** would be ... Process Control **Memory** Alloc. ... only 10% of BTB misses, 18% of data **cache misses**, 9% of ...  
[Cited by 46](#) - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

MPS: Miss-Path Scheduling for Multiple-Issue Processors - group of 11 »

S Banerjia, SW Sathaye, KN Menezes - MPS, 1998 - doi.ieeeecs.org  
 ... fits the equation Time to schedule = **memory** latency + # instructions ... SW Sathaye is with the **IBM TJ Watson** ... PM Mills and BA Patel , "**Optimization** of Instruction ...  
[Cited by 11](#) - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

Power analysis of embedded operating systems - group of 19 »

RP Dick, G Lakshminarayana, A Raghunathan, NK Jha - Design Automation Conference, 2000. Proceedings 2000. 37th, 2000 - ieeexplore.ieee.org  
 ... a system- atic approach to RTOS power modeling and **optimization**. ... inter-procedure communica- tion through the use of shared **memory**. ... [7] **IBM**, 1995 DRAM Databook. ...  
[Cited by 54](#) - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

Exploiting Instruction-Level Parallelism for **Memory** System Performance - group of 7 »

VS Pai - 2000 - 129.215.96.3  
 ... was also supported by **IBM** Corporation, Intel Corporation, the National ... **Memory** system ...  
 mance, so **optimization** approaches that target this subsystem are becoming ...  
[Cited by 2](#) - [Related Articles](#) - [View as HTML](#) - [Web Search](#)

Thread-sensitive scheduling for smt processors - group of 9 »

S Parekh, S Eggers, H Levy... - University of Washington Technical Report, 2000 - navet.ics.hawaii.edu  
 ... **IBM TJ Watson** Research Center sujay@us.ibm.com ... simulator that models the entire **memory** hierarchy ... which targets a different processor resource for **optimization**. ...  
[Cited by 32](#) - [Related Articles](#) - [View as HTML](#) - [Web Search](#)

Google ►

Result Page: 1 2 [Next](#)

ibm memory optimization profiling st

[Google Home](#) - [About Google](#) - [About Google Scholar](#)

©2007 Google



## Redbook publications results

### Refine your results

Category: All Redbooks / Redpapers [[change category](#)]

Search term: rp3 "memory optimization" "cache misses" [[new search](#)]

Select an attribute or enter a search term to refine your results:

#### Category

- [Applications - Desktop & Enterprise](#)
- [Application Servers](#)
- [BladeCenter](#)
- [Business Integration](#)
- [Commerce](#)
- [Data & Information Management](#)
- [Linux](#)
- [Messaging Applications](#)
- [Networking](#)
- [Organizational Productivity, Portals & Collaboration](#)
- [Software Development](#)
- [Storage hardware, TotalStorage](#)
- [Storage Management](#)
- [System i, AS/400](#)
- [System p, RS/6000](#)
- [Systems Management](#)
- [System x](#)
- [System z, S/390](#)
- [Windows](#)
- [Other \(Grid, autonomic computing and more\)](#)

#### Publish date

[Last month](#) | [Last 3 months](#) | [Last 6 months](#) | [Last 12 months](#)

Search within results:  Search

1 - 10 of 88 results\* | [Next](#) ➤

Publish date

Sort by: Date - oldest first Go

1. [\*\*Redbook - Evaluating "EXPLORE for VSE" In a VM/VSE Environment\*\*](#) 1994-09-16  
This document evaluates the usage of EXPLORE for VSE and EXPLORE for CICS in a VM/VSE environment. Its main purpose is to explain which values provided by EXPLORE for VSE are usable if VSE/ESA is running under VM/ESA and not native on the hardware. VMPRF was used to look at the VSE/ESA virtual machine from the VM/ESA side and to compare EXPLORE for VSE and related VMPRF values if applicable. In addition it provides information about the installation of EXPLORE for VSE and EXPLORE for CICS in a VM/VSE environment. This document was written for technical professionals who are evaluating VM/ESA and VSE/ESA performance. A good knowledge of VM/ESA and VSE/ESA is assumed.
2. [\*\*Redbook - Understanding Performance Tuning Theory for IBM OS/2 LAN Server\*\*](#) 1994-11-06  
This document provides the performance information for LAN Server Version 3.0 and 4.0 products. This covers the detail description of LAN Server's mechanism including SMB protocols and buffering logics.



3. **Redbook - IBM PC Server Disk Subsystem Configuration and Sizing** 1995-11-07  
This document provides detailed information on how to select the right server system for your business needs and how to optimal configure the disk subsystem in IBM PC Server products. The document provides example configurations as well as reference material on the IBM PC Server disk subsystem.
4. **Redbook - OS/390 Release 2 Implementation MVS, SMP/E, SDSF, and RMF** 1997-01-22  
This redbook describes the new functions in OS/390 Release 2. It was written for systems programmers who need to understand these functions and the considerations for implementing them. Several practical examples are presented to demonstrate the use of these new functions. Some knowledge of OS/390 and MVS/ESA is assumed. The OS/390 Release 2 ServerPac installation process is described by showing the process steps used in the installation of the ITSO OS/390 Release 2 system. An enhancement for up to 10 additional data sets may be concatenated to SYS1.PARMLIB at IPL. An installation may, if desired, dynamically change the logical parmlib by switching to another set of parmlib data sets through use of a new operator command. New enhancements have been made in LNKST and LPALST. In addition, a parmlib symbolic pre-processor tool, which is an ISPF-based interactive dialog, is available to show you what your system symbolics and parmlib members would be, given a hypothetical hardware and software configuration. A new enhancement to Global Resource Serialization uses a star topology as an alternative to the current ring implementation. A check list is provided that makes an inventory of the analysis and activities to be followed while planning a migration to a GRS star configuration. An appendix describes a tool that monitors supervisor calls 56 and 48 (ENQ/RESERVE/DEQ) and collects data about the resources serialized and the requesters. Also, an appendix describes a sample exit ISGGREX0 based on the ISGGREXS
5. **Redbook - IBM 2210 Nways Multiprotocol Router Description and Configuration Scenarios - Volume 1** 1997-06-20  
This redbook describes the IBM 2210 Nways Multiprotocol Router and its operating software, the Nways Multiprotocol Routing Services (MRS). It provides a technical overview of functions implemented by the IBM 2210 such as bridging, multiprotocol routing, data link switching, frame-relay boundary access node and LAN Network Manager support. One chapter is dedicated to the important special features implemented by the IBM 2210, such as WAN Restoral, WAN Reroute, Dial-on-Demand, Bandwidth Reservation, and EasyStart. The redbook also contains practical scenario descriptions and implementation, showing details of the topology and the commands entered in the console of the IBM 2210. This redbook will help you build a routing environment using the IBM 2210 Nways Multiprotocol Router. With detailed step-by-step implementation of various scenarios, this redbook can be used as a sample when configuring not only the basic routing but also all the additional special features available in this product. Some knowledge of networking architectures and protocols is assumed.
6. **Redbook - OS/390 MVS Parallel Sysplex Capacity Planning** 1998-01-08  
Capacity planning in the Parallel Sysplex environment must address specific transition and growth considerations. Opportunities exist for balancing your workload across systems in a Parallel Sysplex. Resources such as systems, Coupling Facilities and links belonging to a Parallel Sysplex have a finite capacity which, when exhausted, may slow down or disrupt service to users. You can avoid these conditions and significantly increase the productivity of

users by careful capacity planning. This redbook provides an overview of capacity planning. It defines the process and the vocabulary, and provides detailed explanations about how to do capacity planning in the Parallel Sysplex environment. Related IBM tools that help in this process are also discussed. Capacity planning considerations for OS/390 V2R4 and related subsystems such as the DB2, IMS/DB and CICS/VSAM RLS data sharing environments are included. For the DB2 environment, a methodology is outlined for estimating the CF locking rates and for obtaining locking information based on DB2PM reports from your current system. A detailed description of RMF reporting for a Parallel Sysplex is provided. Case studies are included for Quick-Sizer modelling of DB2 and IMS/DB data sharing. These case studies are constructed so that you can try them while reading the redbook. Additionally, information and case studies are included for UNIX capacity planning in a S/390 environment. A discussion and case study are included for a CF processing model, which enables you to e

7. **Redbook - AS/400 Communication Performance Investigation - V3R6/V3R7** 1998-01-13

Improving communication performance is not a trivial task. The purpose of this redbook is to discuss how to manage communications performance and ways to locate the problem areas in communication performance. This redbook collects a large amount of the performance information from several sources and presents it in an ordered manner. The databases created by the Performance Tools/400 were used to give the key performance indicators. This redbook is intended for technical professionals including network designers who want to tune the IBM AS/400 system to improve communications performance. An intermediate knowledge of the Performance Tools/400 (5716-PT1) and Query/400 (5716-QU1) is assumed.

8. **Redbook - Consolidating UNIX Systems onto OS/390** 1998-06-04

This redbook describes the IBM S/390 Enterprise Server as a target for the consolidation of applications currently running on multiple distributed UNIX servers. The objectives of the book are: to show how server consolidation is economically justified in many situations, to position S/390 within the spectrum of consolidation offerings, to show that S/390 should be the platform of choice for selected environments and, to provide some practical guidance in the planning and execution of a project to consolidate multiple UNIX servers onto OS/390.

9. **Redbook - IBM Versatile Storage Server** 1998-08-21

This redbook gives a broad understanding of the new architecture of the Versatile Storage Server (VSS). This book provides an introduction, and describes in detail the architecture, technology, data flow, configuration, migration and recovery aspects for the VSS.

10. **Redbook - RS/6000 Scientific and Technical Computing: POWER3 Introduction and Tuning Guide** 1998-09-18

This redbook provides information to help you understand and exploit the new generation of computer systems based on the RS/6000 POWER3 architecture. Specifically, this publication will address the following issues: POWER3 features and capabilities CPU and memory optimization techniques, especially for Fortran programming AIX XL Fortran Version 5.1.1 compiler capabilities and which options to use Parallel processing techniques and performance Available libraries and programming interfaces Performance examples on commonly used kernels and on several full applications The anticipated audience for this redbook is as follows: Application developers End users who